(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 585 788 A1**

US 5,285,369

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: 93113538.8

(51) Int. Cl.5: **H02M 3/335**

(22) Date of filing: 25.08.93

(30) Priority: 01.09.92 US 938703

(43) Date of publication of application: 09.03.94 Bulletin 94/10

(84) Designated Contracting States: DE FR GB IT NL SE

(71) Applicant: POWER INTEGRATIONS, INC.
411 Clyde Avenue
Mountain View, CA 94043(US)

(72) Inventor: Balakrishnan, Balu
20745 Granada Court
Saratoga, CA 95070(US)

(74) Representative: Blumbach Weser Bergen Kramer Zwirner Hoffmann Patentanwälte
Sonnenberger Strasse 100
D-65193 Wiesbaden (DE)

(54) **Switched mode power supply integrated circuit with start-up self-biasing.**

(57) An embodiment of the present invention is a switching power supply that includes a full-wave bridge rectifier to rectify incoming AC line voltage, a transformer having a primary winding and two secondary windings and a switched mode power supply chip that includes an integrated high voltage power MOSFET with a low voltage tap in the drift region. The MOSFET controls power switching of the primary winding of the transformer and has a high voltage present during initial power-up. This high voltage is dropped across the JFET part of the MOSFET and supplies a regulator with power either temporarily or continuously to operate a pulse width modulator in the chip that controls the switching of the MOSFET.

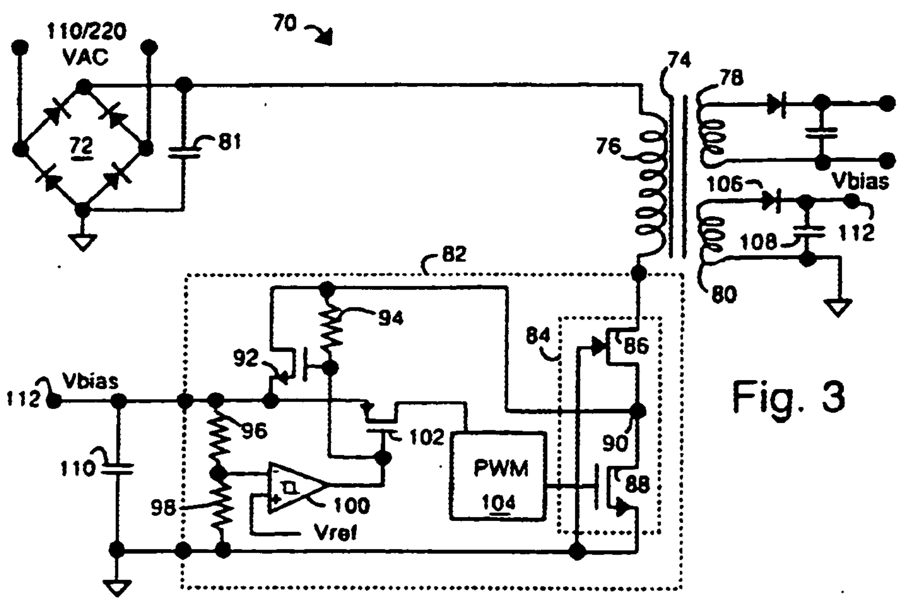


Fig. 3

EP 0 585 788 A1

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electronic switching power supplies and specifically to the integrated circuit devices used in switching power supplies.

2. Description of the Prior Art

The cost to manufacture a power supply is a principal concern in selecting power supply types to be used in particular applications and the components selected to construct them. Switching power supplies have become cost competitive with much simpler linear power supplies because integrated circuit (IC) technology has advanced such that a majority of the complex switch mode circuits can be integrated on a single chip. As a rule of thumb, the fewer necessary pins on an IC package the lower will be the cost. Fewer support components and less expensive peripheral components also will reduce the overall cost of a power supply.

Fig. 1 illustrates a prior art power supply 10 that includes a full-wave bridge rectifier 12, a transformer 14 with a primary winding 16 and a pair of secondary windings 18 and 20, a switched mode power supply chip 22, a plurality of filter capacitors 24-27, a pair of diodes 28 and 30, and a high-voltage high-wattage resistor 32. The power to operate chip 22 is produced by secondary winding 20, diode 30 and capacitor 27 and is referred to as V_{bias}. However, at power start-up, chip 22 will be without power because primary winding 16 will be open and no voltage will be induced into secondary winding 20 because chip 22 is not switching. To initiate such switching, a point with high-voltage DC is tapped on bridge rectifier 12 by resistor 32 and the current is filtered by capacitor 25. This tap will supply just enough current through resistor 32 to start chip 22. Unfortunately, resistor 32 must be a high-wattage type because significant amounts of power can be dissipated in the process of dropping the high voltage of the line to the low voltage required by chip 22. The waste of power is continuous, even after Vbias is available. This problem is particularly severe when input voltage range is wide (e.g., 80-275 VAC for universal operation). Given worst case design rules, resistor 32 has to be designed to provide the required start up current for the lowest expected voltage. Thus, at the highest expected voltage, resistor 32 must dissipate all the more power. To compound the problem, such high-wattage resistor types require extra space and air circulation.

Fig. 2 illustrates a prior art power supply 50 that is similar to power supply 10, except resistor 32 has been eliminated and chip 22 is replaced by a switched mode power supply chip 52. A voltage regulator internal to chip 52 allows the elimination of resistor 32 and includes a high voltage pre-regulator transistor 54, a series-pass transistor 56 and an undervoltage comparator 58. A resistor 60 biases transistor 54 on and during initial power-up, transistor 54 will pull transistor 56 up and supply power to a pulse width modulator (PWM) 62 that switches on a power output transistor 64. A voltage develops across primary winding 16 and induces a voltage in secondary winding 20 which supplies Vbias. With V_{bias} being supplied, comparator 58 operates to maintain transistor 54 off and no further high voltage power is required. Turning off high voltage pre-regulator 54 will save power after start up, but such a function is more expensive to implement, as it requires a high voltage transistor and extra pin with high voltage safety spacing.

The typical prior art high voltage transistor used in the pre-regulator of switch mode power supply chips is usually a relatively small device. The transistor's immunity to line transients is therefore limited. Thus, the pin associated with the transistor becomes a limiting factor for electrical static discharge (ESD) and safe operating area (SOA) rating of the switching regulator chip.

SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide a switched mode power supply chip which does not require a dedicated terminal pin for tapping high voltage during start-up.

Briefly, an embodiment of the present invention is a switching power supply that includes a full-wave bridge rectifier to rectify incoming AC line voltage, a transformer having a primary winding and two secondary windings and a switched mode power supply chip that includes an integrated high voltage power MOSFET with a low voltage tap in the drift region. The MOSFET controls power switching of the primary winding of the transformer and has a high voltage present during initial power-up. This high voltage is dropped across the JFET part of the MOSFET and supplies a regulator with power either temporarily or continuously to operate a pulse width modulator in the chip that controls the switching of the MOSFET.

An advantage of the present invention is that an integrated circuit is provided that does not require a high power bias resistor or a high voltage pre-regulator.

An advantage of the present invention is that an integrated circuit is provided that allows for a simple fully integrated power supply chip that requires few pins and external components.

A further advantage of the present invention is that an integrated circuit is provided that is economic.

Another advantage of the present invention is that an integrated circuit is provided that saves significant power compared to prior art power supplies that use a high-voltage dropping resistor.

An advantage of the present invention is that an integrated circuit is provided that allows for a fully integrated switching power supply with only one high-voltage pin, thus reducing electro-static discharge and safe operating area concerns over prior art implementations that require at least two high-voltage pins.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

IN THE DRAWINGS

Fig. 1 is a schematic diagram of a prior art power supply that includes a high-voltage dropping resistor to generate power-up starting bias;

Fig. 2 is a schematic diagram of another prior art power supply that includes a high-voltage regulator transistor within a power supply chip to generate power-up starting bias;

Fig. 3 is a schematic diagram of a switched mode power supply of the present invention; and

Fig. 4 is a diagram of the chip layout of the power supply chip used in the power supply of Fig. 3.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Fig. 3 illustrates a power supply embodiment of the present invention, referred to by the general reference numeral 70. Power supply 70 comprises a full-wave bridge rectifier 72, a transformer 74 with a primary winding 76 and a pair of secondary windings 78 and 80, and a switched mode power supply chip 82. A high voltage power metal-oxide-semiconductor field effect transistor (MOSFET) 84 included within chip 82 comprises the equivalent of a junction field effect transistor (JFET) 86 and an insulated gate FET (IGFET) 88. A tap 90 provides low voltage to a regulator 92 and a resistor 94 when IGFET 88 is off.

MOSFET 84 is preferably similar to that described in United States Patent 4,811,075, issued March 7, 1989, to Klas H. Eklund. An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same semiconductor chip to form a high-voltage MOS field effect transistor. An extended drain region is formed on top of a substrate of opposite conductivity material. A top layer of material, similar to the substrate, is formed by ion implantation through the same mask window as the extended drain region. The top layer covers only a middle part of the extended drain which has ends that meet with a silicon dioxide layer above. Current flow through the extended drain is controlled by the substrate and top layer which pinch-off the extended drain between them in a familiar field-effect fashion. The drift region of MOSFET 84 is used to drop the high line voltage to a low voltage for biasing chip 82. The junction between the JFET 86 and IGFET 88 at tap 90 is limited typically to 15-20 volts, due to the pinch-off action of JFET 86.

A pair of resistors 96 and 98 provide a voltage division for an undervoltage comparator 100 that controls a series pass transistor 102. The output of transistor 102 is an internal low-voltage supply to a pulse width modulator (PWM) 104. Once the internal low-voltage supply comes up, PWM 104 can control IGFET 88 on and off. This will cause transformer 74 to operate and induce a voltage into winding 80. A diode 106 and a pair of capacitors 108 and 110 will provide a smoothed, low-voltage DC referred to as V_{bias}, to a junction 112. JFET 86, which is pinched off, behaves like a current source and provides the current to charge up the bypass capacitor 110. V_{bias} thereafter provides the source for the internal low-voltage supply and transistor 92 may be turned off. When the voltage at junction 112 reaches a required value, the voltage may be regulated by controlling the transistor 92.

As long as IGFET 88 is off each cycle for a time sufficient to provide enough current through JFET 86 to satisfy the average internal low voltage supply current requirement. Chip 82 could be continuously operated from the high voltage line, if that is desired. However, providing the chip supply current from the high voltage line for normal operation causes significant power loss in JFET 86 which can be avoided by using low voltage V_{bias} derived from the transformer output. In this case transistor 92 is turned off when chip 82 is activated after the voltage at junction 112 reaches its operating voltage and the V_{bias} is used to power chip 82. In order for this to work, capacitor 110 has to be large enough to provide the supply current without significant drop in voltage until the V_{bias} comes up. The hysteresis on comparator 100 allows for some voltage subsidence across capacitor 110 during a transition period that exists between transistor 92 turning off and the rise of V_{bias} to its normal operating level. If the voltage across capacitor 110 drops below the hysteresis value before V_{bias} assumes its full value, comparator 100 will switch transistor 92 on and

transistor 102 off, and the start-up cycle will repeat until Vbias is available.

Fig. 4 illustrates a typical chip layout for chip 82. Because MOSFET 84 is a high-voltage, high-current type, the chip real estate required for its implementation is significant. In the prior art example of Fig. 2, high-voltage transistor 54 would also require a significant amount of chip area. Therefore the elimination of such a transistor as high-voltage transistor 54 in the present invention reduces both die size and manufacturing costs.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

Claims

1. A switched mode power supply chip, comprising:
   power switching means for switching a primary winding of a switched mode power supply transformer on and off, the power switching means comprising a first transistor for limiting a voltage applied to a drain of a second transistor;
   a low voltage tap connected to said drain of said second transistor; and
   regulator means for generating a voltage supply from the low voltage tap during a start-up of the chip from a power-off condition that is sufficient to begin operation of the power switching means.

2. The chip of claim 1, wherein:
   the power switching means comprises a MOSFET device and said first transistor is a JFET with a grounded gate and said second transistor is an IGFET with a grounded source.

3. The chip of claim 1, wherein:
   the regulator means comprises a third transistor and a resistor for pulling up a gate of said third transistor and a voltage comparator for maintaining a regulated voltage at a source of said third transistor.

4. The chip Of claim 1, wherein:
   the power switching means comprises a MOSFET device and said first transistor is a JFET with a grounded gate and said second transistor is an IGFET with a grounded source; and
   the regulator means comprises a third transistor and a resistor for pulling up a gate of said third transistor and a voltage comparator for maintaining a regulated voltage at a source of said third transistor.

5. An integrated circuit (IC) with internally generated start-up bias for power-up conditions, the IC comprising:
   power switching means for switching a high voltage output current connected to the IC on and off, the power switching means including a first transistor for limiting voltage applied to a drain of a second transistor;
   a low voltage tap connected to said drain of said second transistor; and
   regulator means for generating a voltage supply from the low voltage tap during a start-up of the chip from a power-off condition that is sufficient to begin operation of the power switching means.

6. A power supply, comprising:
   full-wave bridge rectifier means for producing a high voltage DC from an AC power input;
   filter capacitor means for smoothing said high voltage DC from the full-wave bridge rectifier means;
   transformer means for producing isolated DC output and chip bias voltages from said high voltage DC; and
   integrated circuit means for switching said high voltage DC through the transformer means such that said isolated DC output and chip bias voltages are regulated, the integrated circuit means including:
   a junction field effect transistor (JFET) with a gate connected to a ground of the power supply such that a drain connected to said high voltage DC through the transformer means prevents a voltage equal to said high voltage DC from appearing at a source of said JFET;
   an insulated gate field effect transistor (IGFET) with a source connected to said ground and a drain connected to said source of said JFET;
   pulse width modulator (PWM) means for driving a gate of said IGFET in response to a voltage sampled from said isolated DC output; and
   first voltage regulator means for supplying an operating current to said PWM means from a voltage available at said source of said JFET.

7. The power supply of claim 6, wherein the integrated circuit means further comprises:

second voltage regulator means for supplying an operating current to said PWM means from said isolated chip bias voltage.

8. A switched mode power supply chip, comprising:

power switching means for switching a primary winding of a switched mode power supply transformer on and off, the power switching means comprising a first transistor for limiting a voltage applied to a drain of a second transistor;

a low voltage tap connected to said drain of said second transistor; and

regulator means for generating a voltage supply from the low voltage tap that is sufficient to continuously operate the power switching means.

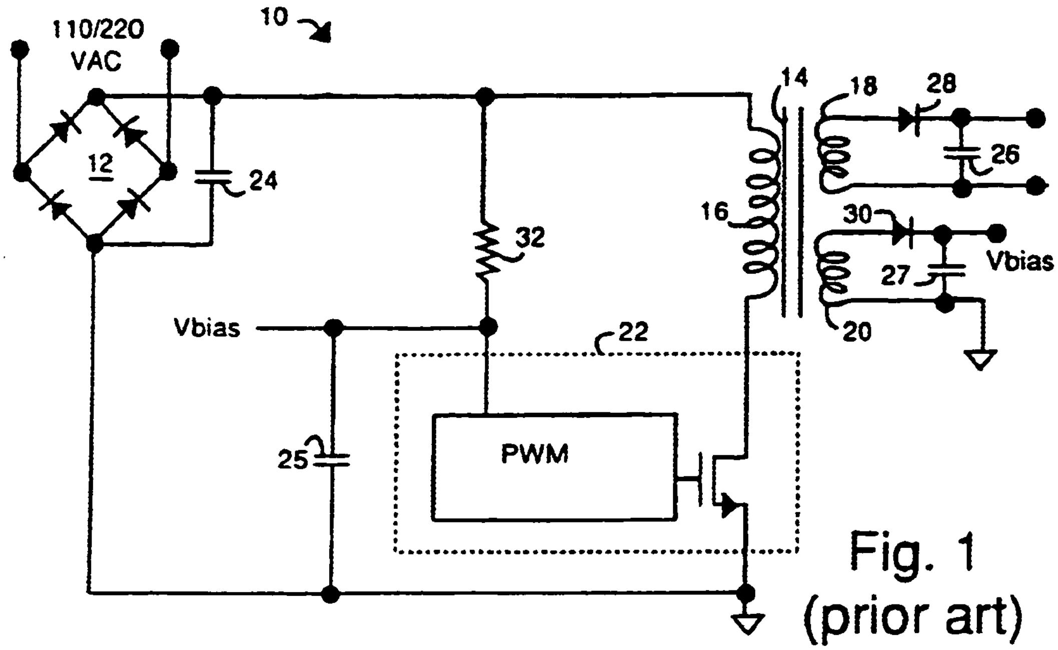


Fig. 1
(prior art)

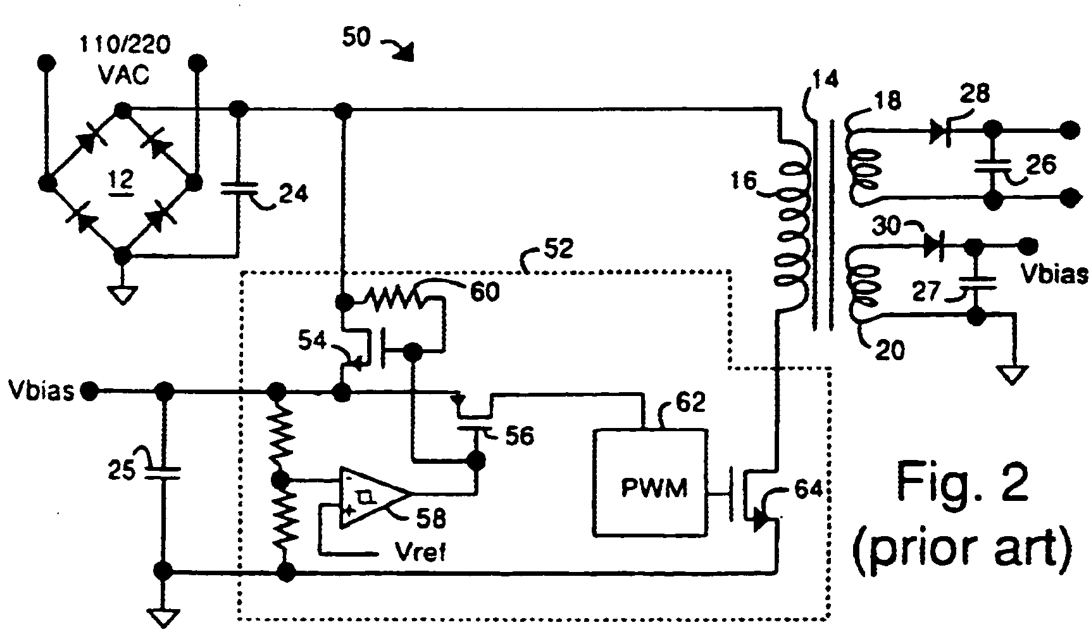
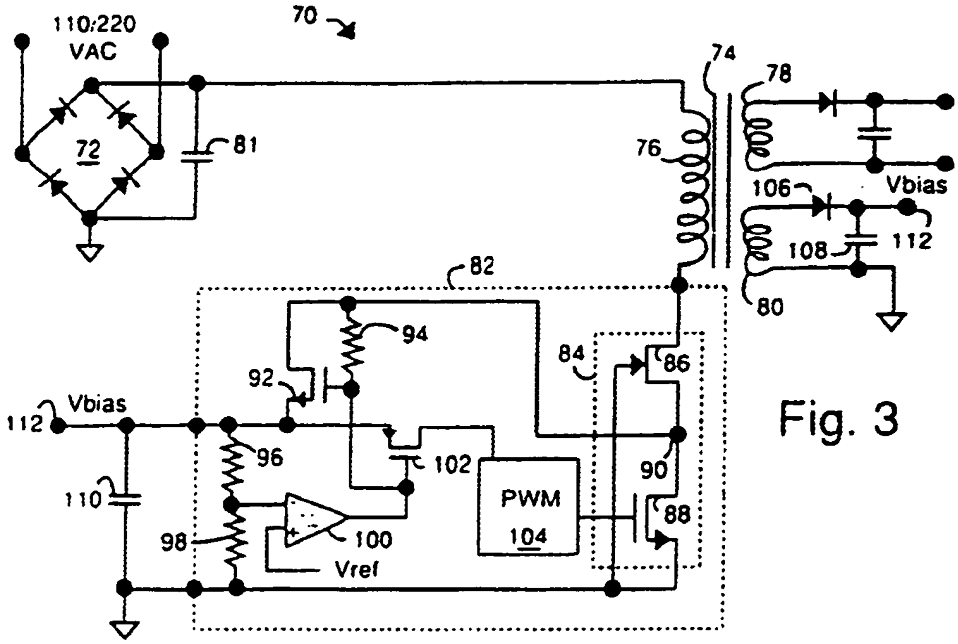
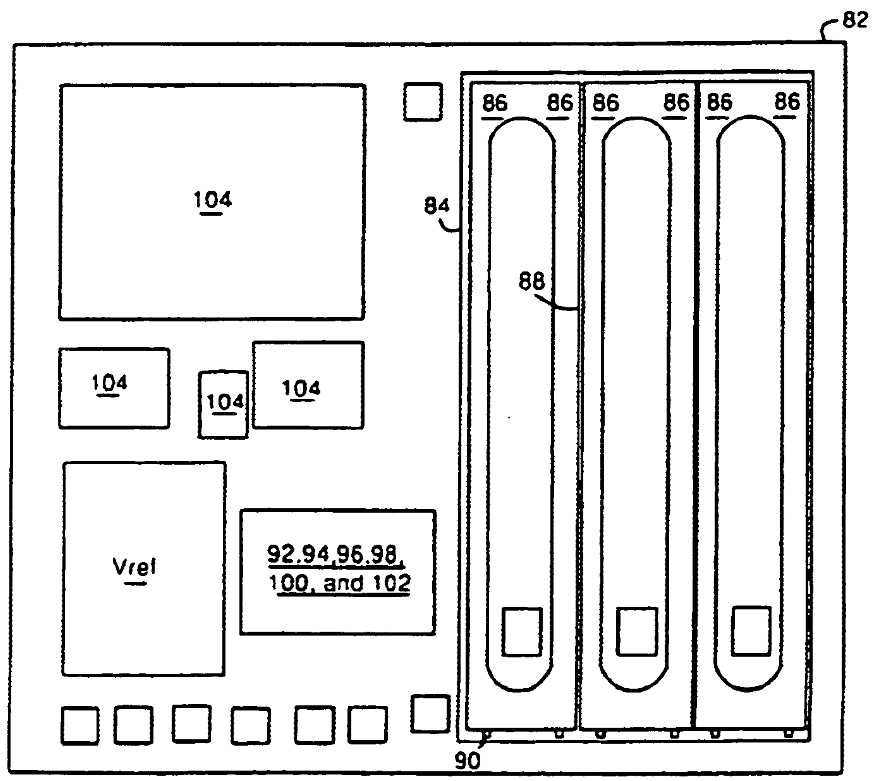


Fig. 2
(prior art)



110/220
VAC
70
72
81
74
78
76
106
Vbias
108
112
80
82
94
84
86
92
Vbias
112
96
102
90
110
PWM
104
88
98
100
Vref

Fig. 3



82
104
86
86
86
86
86
86
84
88
104
104
104
Vref
92,94,96,98,
100, and 102
90

Fig. 4